IN THE SPECIFICATION

The specification as amended below with replacement paragraphs shows added text with underlining and deleted text with ~~strikethrough~~.

Please REPLACE the paragraph numbered [0064] at page 43, with the following paragraph:

[0064] In the case that data is stored in the (P) mode in any one of the cache memories, the cache controller 30 for causing the data to be stored in the (P) mode carries out the following operation through the function of the passive reading mode processing unit 48 shown in FIG. 7 when a request message based on the normal read or the weak protocol read is sent out into the common bus by a memory access request from some other cache devices. First, the state-examination-result based on the request message sent into the common bus 14 is waited. In this case, the cache controller 30 in which the data in the (P) mode is stored does not assert any of the EX line, the HIT line and the HITM line regardless of the state of the cache so that to the other cache controllers appear the invalid state (I) when they are observed from the outside. In the case that any of the ~~Invalid line,~~ EX line, the HIT line and the HITM line is not asserted on the basis of the result of state-examination in the other cache devices, that is, in the case that the cache controllers other than the cache controller for causing the data in the (P) mode to be stored are invalid (I), this controller 30 changes the state of the data in the (P) mode to the invalid state (I) in order to invalidate its own data. In this manner, the other cache controller which issued the read request can read data in the requested address, in the exclusive state (E), from the main memory 18 and cause the data to be stored. In the case that the Ex line or the HITM line is asserted and the data is stored, in the exclusive state (E) or the data-modified state (M), in any one of the other cache devices, the cache controller 30 for causing the data to be stored in the (P) mode changes the state of the data in the (P) mode to the invalid state (I). On the other hand, in the case that the other cache controllers are in the data-shared state (S), wherein the HIT line is asserted, on the basis of the result of the state-examination of the other controllers the cache controller 30 for causing the data in the (P) mode to be stored does not need to change its own data.